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### ⑳ Method for producing a semiconductor device.

㉑ A method for producing a semiconductor device comprises the steps of: forming an insulating layer (13) on a semiconductor substrate (11) provided with an electrode portion (12), forming a barrier metal layer (16) over the surface, forming a groove (18) in the barrier metal layer (16) so that the groove surrounds the electrode portion (12), introducing a stopper material (20) in the groove (18), forming a bump (22) on the barrier metal layer (16b) positioned on the electrode portion (12), and removing the barrier metal layer (16a) outside of the stopper (22). The stopper material (20) prevents the removal of the inside barrier metal layer (16b) during the removal of the outside barrier metal layer (16a).

Fig. 2B

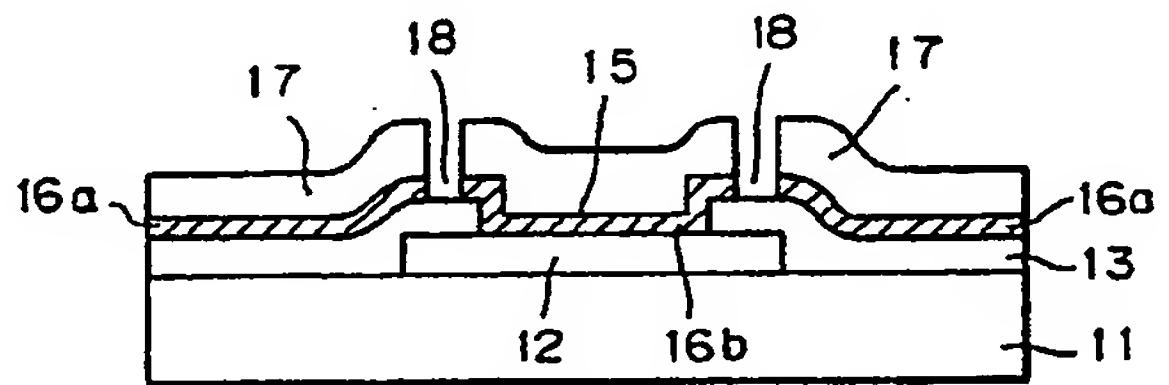
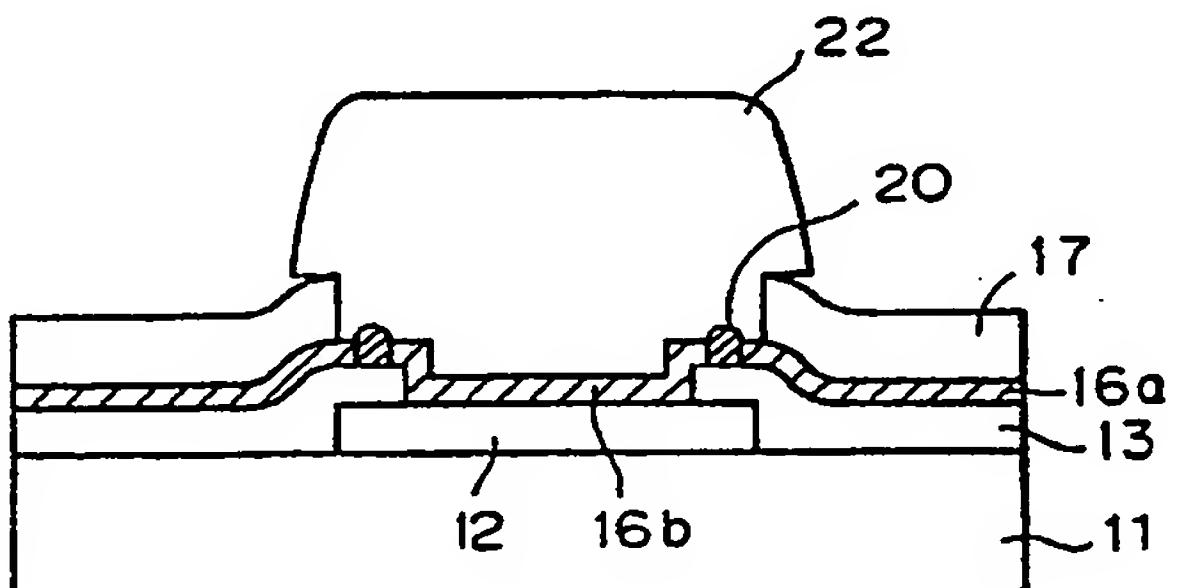


Fig. 2D



EP 0 261 799 A1

### Method For Producing A Semiconductor Device

The present invention relates to a method for producing a semiconductor device. More particularly, it relates to a method for producing a semiconductor device having a metal bump which is used as a terminal electrode.

The terminal electrodes of a semiconductor device are usually formed by, for example, an Au wire terminal electrode. However, the electrode structure wherein a large metal projection or bump is adhered to the electrode portion of the semiconductor device, and wires are connected to the projecting metal, is known.

Since the semiconductor device having the bump does not require wire bonding, the thickness of the package of the semiconductor device is reduced and the size of the bonding pad (electrode region) of a semi-conductor chip is made considerably smaller. Accordingly, a semiconductor device having a bump has an advantage in that it can be assembled in an IC card in a flat shape package and the size of the semiconductor per se is considerably reduced. Further, since a composite device is formed by providing a plurality of semiconductor chip electric circuits, it can be packaged with a high degree of density. Nevertheless, the metal bump per se must have a good adhesion to an electrode.

A method for producing such a semiconductor device comprises the steps of:

forming an insulating layer on a semiconductor substrate provided with an electrode portion,

forming a barrier metal layer over its entire surface,

forming a bump on the barrier metal layer positioned over the electrode portion, and

removing the barrier metal layer using the bump as a mask.

According to this invention such a method comprises the additional steps of:

forming a groove in the barrier metal layer so that it surrounds the electrode portion, and

filling the groove with a stopper material, the stopper material, preventing removal of the barrier metal layer inside the stopper material filled groove during the removal of the barrier metal layer outside the groove.

An advantage of the present invention is that it provides a method for producing a semiconductor device wherein the bump is firmly connected to the electrode or wiring and it is formed with improved reliability.

Layers of Ti having thickness of 100 Å, Cu having a thickness of about 2 µm, and Ni having a thickness of about 1000 Å are preferably used as the barrier metal layer. The width of the groove is

determined by the etching-proof properties thereof and the required bump size, etc. The width of the groove determines the width of stopper material, and large width of the stopper material increases the stopper function. However, if the width of the stopper is too large, the process of plating the stopper material becomes difficult.

Examples of methods in accordance with this invention will now be described and contrasted with the prior art with reference to the accompanying drawings, in which:-

Figures 1A to 1E are cross-sectional views for explaining a conventional method of producing such a semiconductor device;

Figures 2A to 2E are cross-sectional views explaining the steps in a first example of the present invention;

Figure 3 is a plan view of Figure 2C;

Figures 4A to 4C, and Figure 5, show cross-sectional views explaining the steps in a second and third example of the present invention;

Figure 6 is a schematic plan view of Figure 4A;

Figures 7A to 7D are cross-sectional views explaining the steps in a fourth example of the present invention;

Figure 8 is a schematic plan view of Figure 7A;

Figures 9A to 9B are cross-sectional views explaining the steps in a fifth example of the present invention; and,

Figures 10A to 10B are cross-sectional views explaining the steps in a sixth example of the present invention.

Figures 1A to 1E are cross-sectional views explaining a conventional method for providing the above-mentioned device.

As shown in Figure 1A, an aluminium electrode 2 is provided on a semiconductor substrate 1 and a phosphosilicate glass (PSG) film 3 is formed over the substrate 1 and the aluminium electrode 2 by a chemical vapour deposition (CVD) process. A silicon dioxide ( $SiO_2$ ) film may be used instead of the PSG film 3.

Then, as shown in Figure 1B, a first resist film is coated on the PSG film 3, and exposed and developed to form a first resist pattern 4 having an opening at a required position above the electrode 2. The PSG film 3 is then etched, using the resist film pattern 4 as a mask, so that an opening 5 is formed above the electrode 2.

The resist film pattern 4, is then removed, as shown in Figure 1C, and a barrier metal film 6 about 3  $\mu\text{m}$  thick and consisting of three layers of titanium (Ti), copper (Cu), and nickel (Ni) respectively, is formed on the exposed PSG film 3 and electrode 2 by a sputtering process.

Then, as shown in Figure 1D, a second resist film is coated on the barrier metal film 6, and exposed and developed so that a second resist film pattern 7 having an opening larger than the opening 5 is formed at the opening 5. Then, a solder (PbSn) bump 8 is formed at the opening 5 by a plating method using the resist film pattern 7 as a mask. During the plating, the barrier metal film 6 is used as a plating conductive layer.

Then, as shown in Figure 1E the resist film pattern 7 and the exposed barrier metal film 6 are removed, using the solder bump electrode 8 as a mask, by a wet etching method using a mixture of nitric acid and phosphoric acid to remove the nickel and copper, and phosphoric acid to remove the titanium. The wet etching method is used because a dry etching will cause the bump electrode to be easily etched.

Subsequently, the solder bump is melted by a heat treatment to form a semi-spherical bump 8 having a diameter of about 150  $\mu\text{m}$ . A gold (Au) bump may be formed instead of the solder bump, by a method similar to the above-mentioned process.

In the above mentioned method for forming the bump 8, the barrier metal film 6 is interposed between the electrode 2 and the bump 8 so that the bump 8 does not react with the electrode 2. Also the barrier metal film is used as a plating conductive layer, as explained above.

In the etching of the barrier metal film 6 using the solder bump 8 as a mask, a side etching is carried out in a lower portion of the bump 8 as shown in Figure 1D, since in the lower portion of the bump, the flow of the plating liquid becomes uneven and an electrolytic corrosion may occur between the bump 8 and the barrier metal films 6. This deteriorates the adhesive properties between the bump 8 and the aluminium electrode 2, and the bump 8 can be easily separated from the etched barrier metal film 6.

Figures 2A to 2E are cross-sectional views explaining the steps in a first example of the present invention.

The structure shown in Fig. 2A is formed by the same steps as shown in Figs. 1A to 1C for producing a conventional semiconductor device. Then, according to the present invention, a second resist film is formed on a barrier metal film 16 and patterned to form a second resist pattern 17 having a groove 18, as shown in Fig. 2B. In Figs. 2A to 2E, reference numerals 11, 12, 13, and 15 show a

semiconductor substrate, an aluminum electrode, a PSG film, and an opening, respectively. The region inside the groove 18 is bump region on which a bump is to be formed, and is hereinafter called a bump formation region.

As shown in Fig. 3, the groove 18 is formed so that it surrounds the bump formation region, and therefore, the barrier metal film 16b in the bump formation region is not electrically connected to the barrier metal film 16a positioned outside the groove 18.

Then, as shown in Fig. 2C, an electroplating process is carried out, using the barrier metal 16a as a cathode, so that, for example, gold (Au) 20, is buried in the groove 11. In the first stage of the electroplating, the deposition of the gold 20 is started from the end of the barrier metal 16a and expanded to reach the barrier metal 16b, so that the barrier metal 16b is connected to the barrier metal 16a. The plating is advanced then expanded to cover the entire cross section of the groove 18. The width of the groove 18 is preferably about 5  $\mu\text{m}$ . A resist pattern 17 is then formed so that the region except for a bump formation region is masked. Then, as shown in Fig. 2D a mushroom-shaped bump 14 is formed on the barrier metal 16b and gold 20 by a plating process.

Finally, as shown in Fig. 2E, the resist pattern 14 and the barrier metal 16a are removed by an etching process. During this etching of the barrier metal 16a, although the bump 22 is slightly etched at the side thereof, further etching of the bump 22 is stopped by the gold 20. Namely, the gold 20 acts as a stopper.

Figures 4A to 4C and Fig. 5 are cross-sectional views explaining the steps in a second and a third example of the present invention, and Figure 6 is a schematic plan view relating to Figure 4A.

In the second example as shown in Figs. 4A to 4C, a part of the barrier metal layer 16 is not etched during the etching of the barrier metal layer 16, so that the remaining barrier metal layer 16 can be used as an electric path.

As shown in Fig. 4A the barrier metal layer 16 is formed by two layers 16c of Ti and 16d of Pd or Ni/Cu.

When a groove is formed by using the resist pattern 17, only the Pd or Ni/Cu layer is removed and the Ti layer remains. Then, as shown in Fig. 4B, a stopper 24 of Au or solder is plated in the groove 18, and as shown in Fig. 4C, a bump 22 is formed by a plating process at a non-masked position. Finally, the resist pattern 17 and the exposed barrier metal 16d and 16c are removed by an etching process. The stopper 24 prevents etching of the inside barrier metal 16 during this process.

Note, the process shown in Fig. 4B may be omitted. Namely, after forming a groove 18 as shown in Fig. 4A, the bump 22 can be plated by using the resist pattern 17 as a mask, since an electric path is formed by the Ti layer 16c. Thus, the bump metal is buried in the groove 18 of the barrier metal 16c and the buried metal acts as a stopper.

Figures 7A to 7D show cross-sectional views explaining the steps in a fourth example of the present invention.

In this example, after forming the structure having a groove 18 shown in Fig. 2B, the resist film pattern 17 is removed.

Then as shown in Fig. 7A a solder film 25 about 5  $\mu\text{m}$  thick is formed over the entire surface by a vapour deposition process. Subsequently, as shown in Fig. 7B, a resist pattern film 26 is formed only above the aluminum electrode 12, and the solder film 25 is etched using the resist film pattern 26 as a mask. The etching process is carried out by a wet etching using a mixture of ethylene diamine tetra acetic acid, hydrogen peroxide, and ammonia.

The resist film pattern 26 is then removed, as shown in Fig. 7C, and a resist is formed over the entire surface and patterned to form a resist film pattern 27 in such a way that the opening 15 appears only over the aluminum electrode 12. Then, a solder bump 28 having a thin thickness of about 100  $\mu\text{m}$  is formed on the solder film 25 by plating. In the plating process, the barrier metal film 16 and the solder film 25 are used as conductive layers for the electroplating.

Then, the resist film pattern 27 is removed, as shown in Fig. 7D, and an exposed barrier metal film 16 is removed by etching. During this etching, the solder film 25 in the groove 18 acts as stopper.

Finally, the structure is heated at 400°C and the solder bump 22 is completed.

Figures 9A and 9B are cross-sectional views explaining the steps in a fifth example of the present invention.

In the fifth example shown in Figs. 9A and 9B the bump plating is carried out twice. Then as shown in Fig. 2B, after the groove is formed, the resist film pattern 17 is removed.

Then, as shown in Fig. 10A, a bump film 29 is formed and patterned so that the bump film 29 is formed only above an aluminum electrode 12, by using a resist 30. Gold may be used as the bump film material. The thickness of the bump film 29 may be very thin if the bump film 29 is to be used as an electric path in the subsequent bump plating process.

Then, as shown in Fig. 9B, the resist 30 is removed and the bump 31 is plated. Since in this plating the entire bump film 29 becomes a cathode, the bump 31 is thickly formed.

Figs. 10A to 10B are cross-sectional views explaining the steps in a sixth example of the present invention.

The structure shown in Fig. 2B is formed, and then a resist pattern 32 is formed and a bump 31 is plated as shown in Fig. 10A. The outer end of the barrier metal 16 is surrounded by a leg 31a of the bump 31. Therefore, even if the leg 31a of the bump 31 is slightly melted during the etching of the barrier metal 32, as shown in Fig. 10B, the barrier metal 32 is not etched because the leg 31a acts as a stopper.

### Claims

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1. A method for producing a semiconductor device comprising the steps of:

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forming an insulating layer (13) on a semiconductor substrate (11) provided with an electrode portion (12),

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forming a barrier metal layer (16) over its entire surface,

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forming a bump (22) on the barrier metal layer (16) positioned over the electrode portion (12), and

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removing the barrier metal layer (18) using the bump (22) as a mask,

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characterised by the additional steps of:

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forming a groove (18) in the barrier metal layer (16) so that it surrounds the electrode portion (12), and

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filling the groove (18) with a stopper material (20), the stopper material (20), preventing removal of the barrier metal layer (16b) inside the stopper material filled groove (18) during the removal of the barrier metal layer (16a) outside the groove (18).

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2. A method according to claim 1, wherein the insulating layer (13) is composed of phospho-silicate glass or silicon dioxide.

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3. A method according to claim 1 or 2, wherein the electrode portion (12) is composed of aluminum.

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4. A method according to any one of the preceding claims, wherein the barrier metal layer (16) is composed of layers of titanium, copper and nickel.

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5. A method according to any one of the preceding claims, wherein the groove (18) is formed by wet-etching the barrier metal layer (16).

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6. A method according to any one of the preceding claims, wherein the stopper material (20) is formed by fusing gold or solder in the groove (18).

7. A method according to any one of claims 1 to 5, wherein the stopper material (20) introduced into the groove (18) by a plating process.

8. A method according to any one of claims 1 to 5, wherein the stopper material (20) is introduced into the groove (18) by the steps of:

forming a bump layer (25) on the barrier metal layer (16) and filling the groove (18) by plating with the bump material,

removing the barrier metal layer (16) positioned outside the groove (18).

9. A method according to claim 7 or 8, wherein the bump (22) includes a depending leg portion (31a) which fills the groove (18) to form the stopper material.

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Fig. 1A

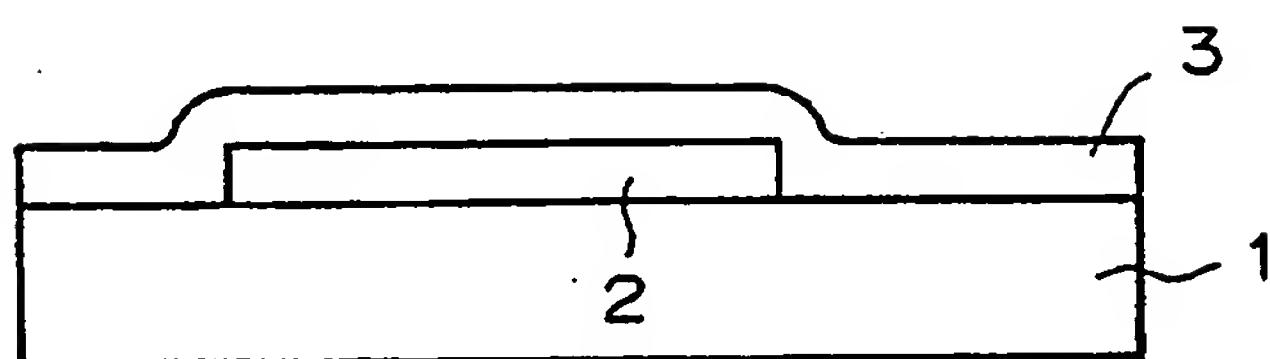


Fig. 1B

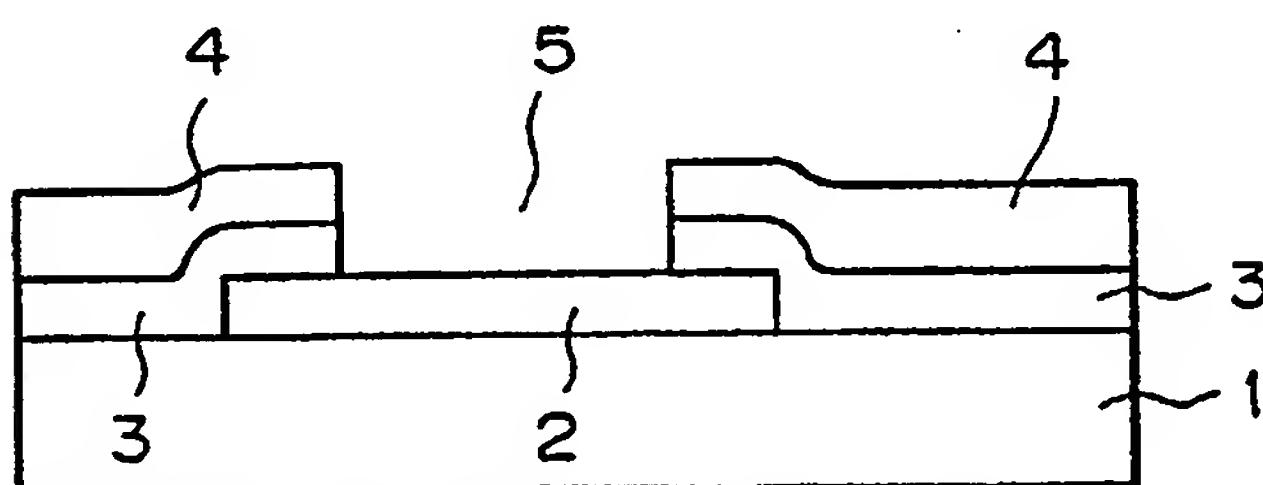


Fig. 1C

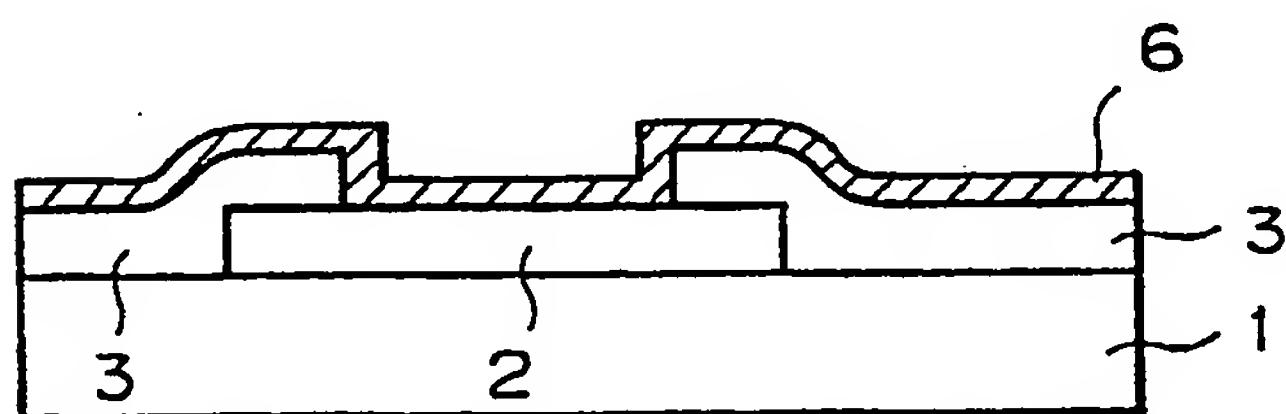


Fig. 1 D

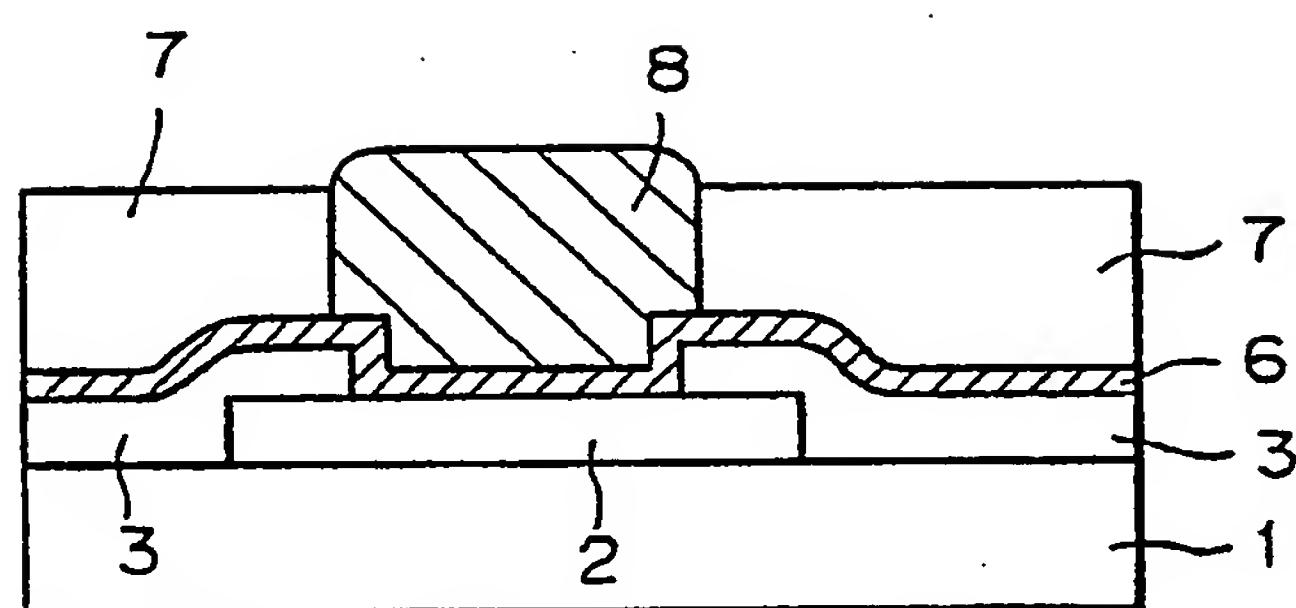


Fig. 1 E

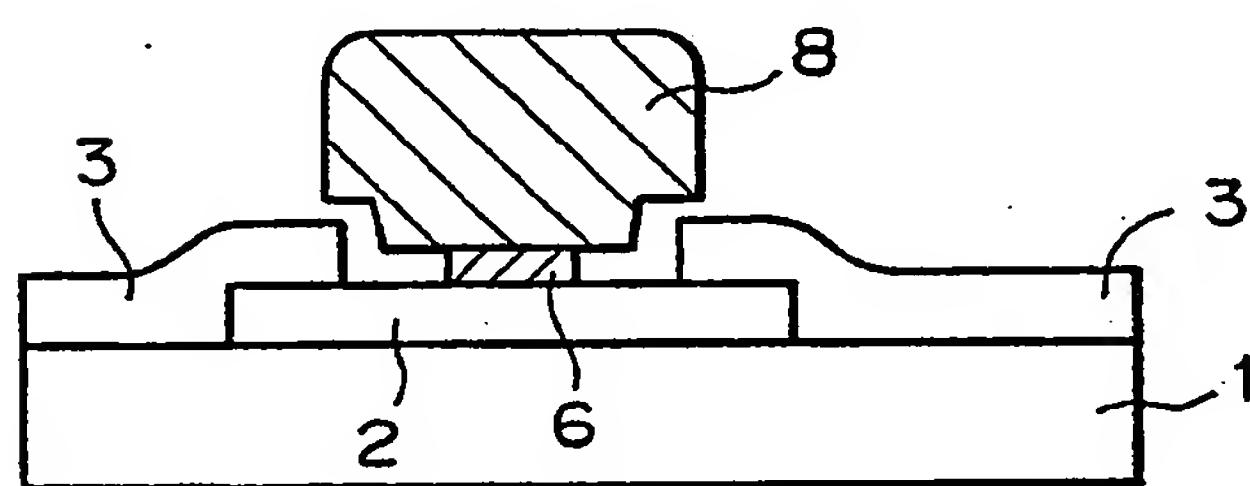


Fig. 2A

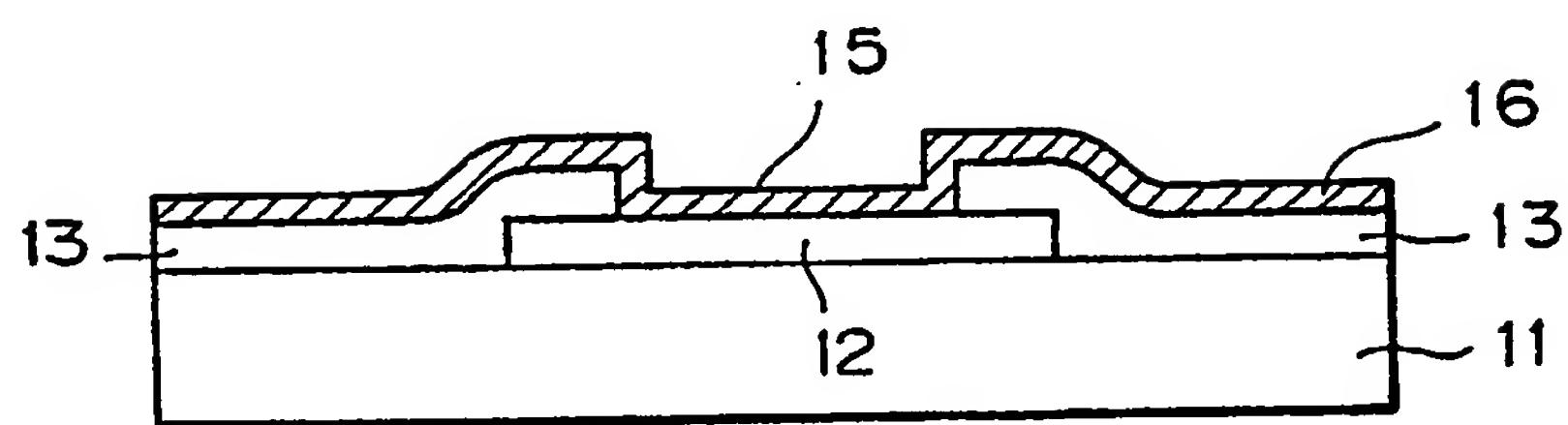


Fig. 2B

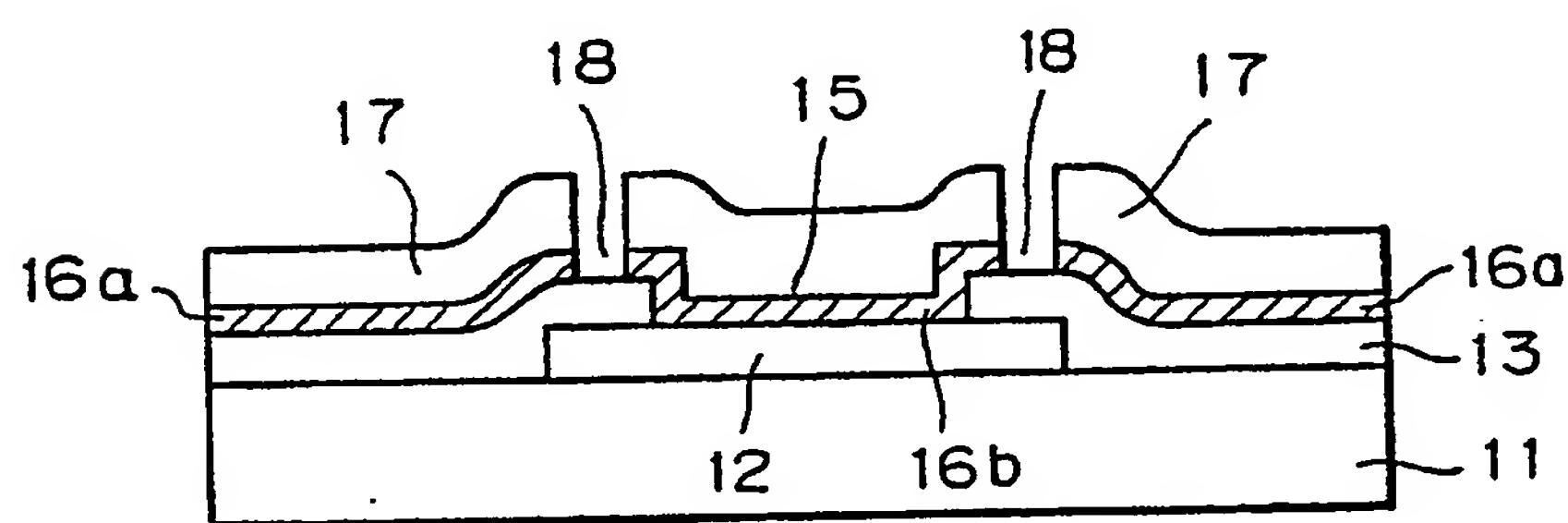


Fig. 2C

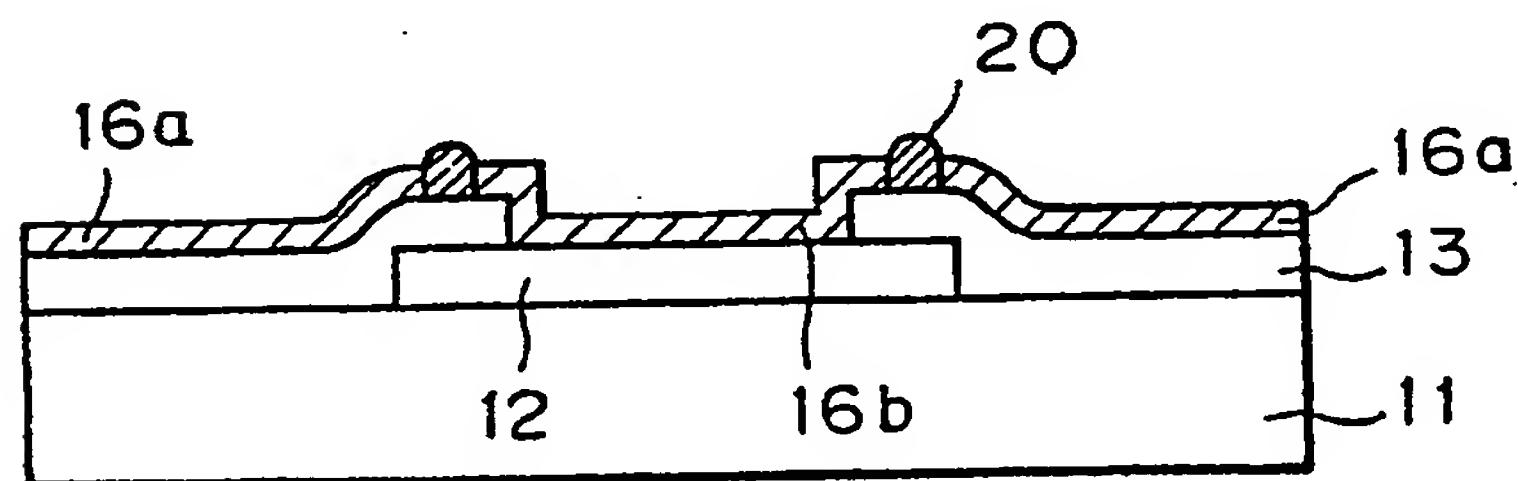


Fig. 2D

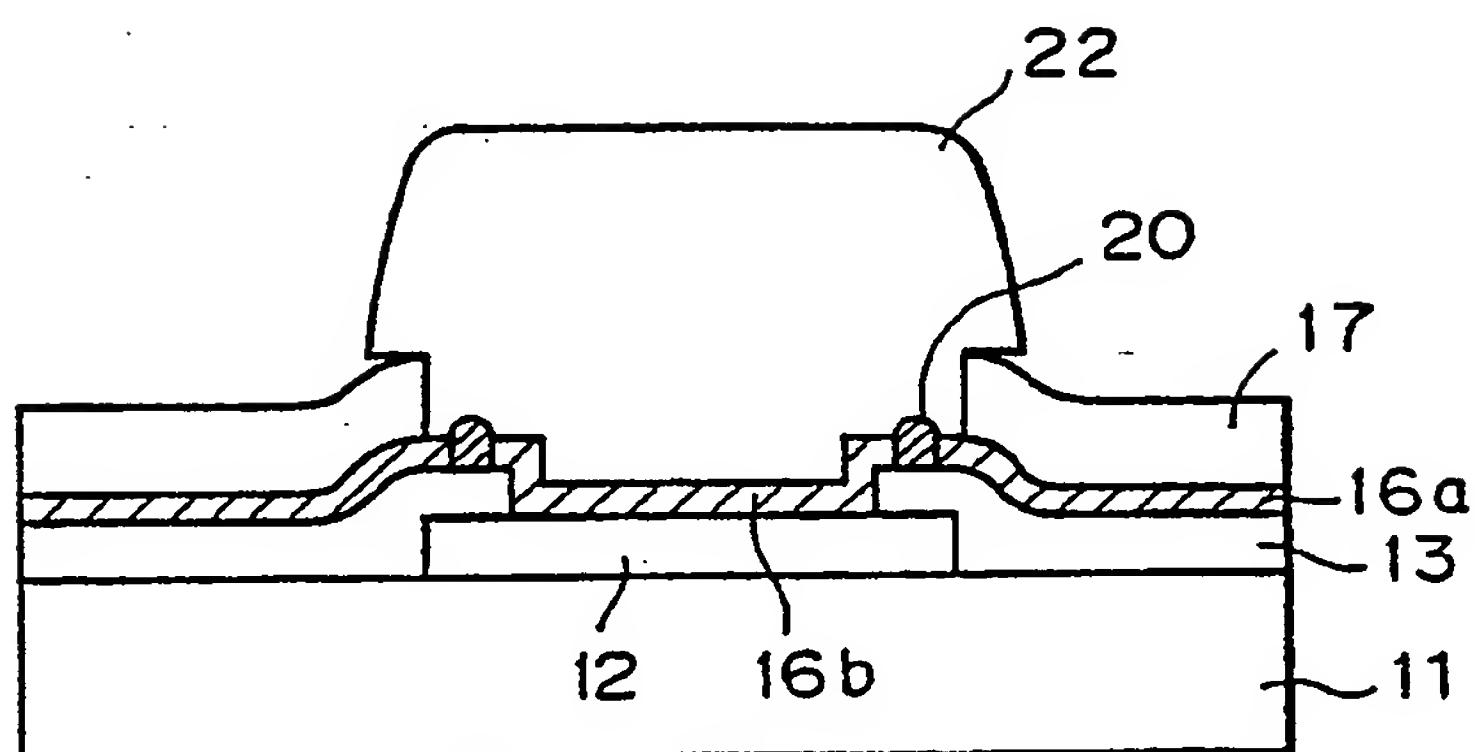


Fig. 2E

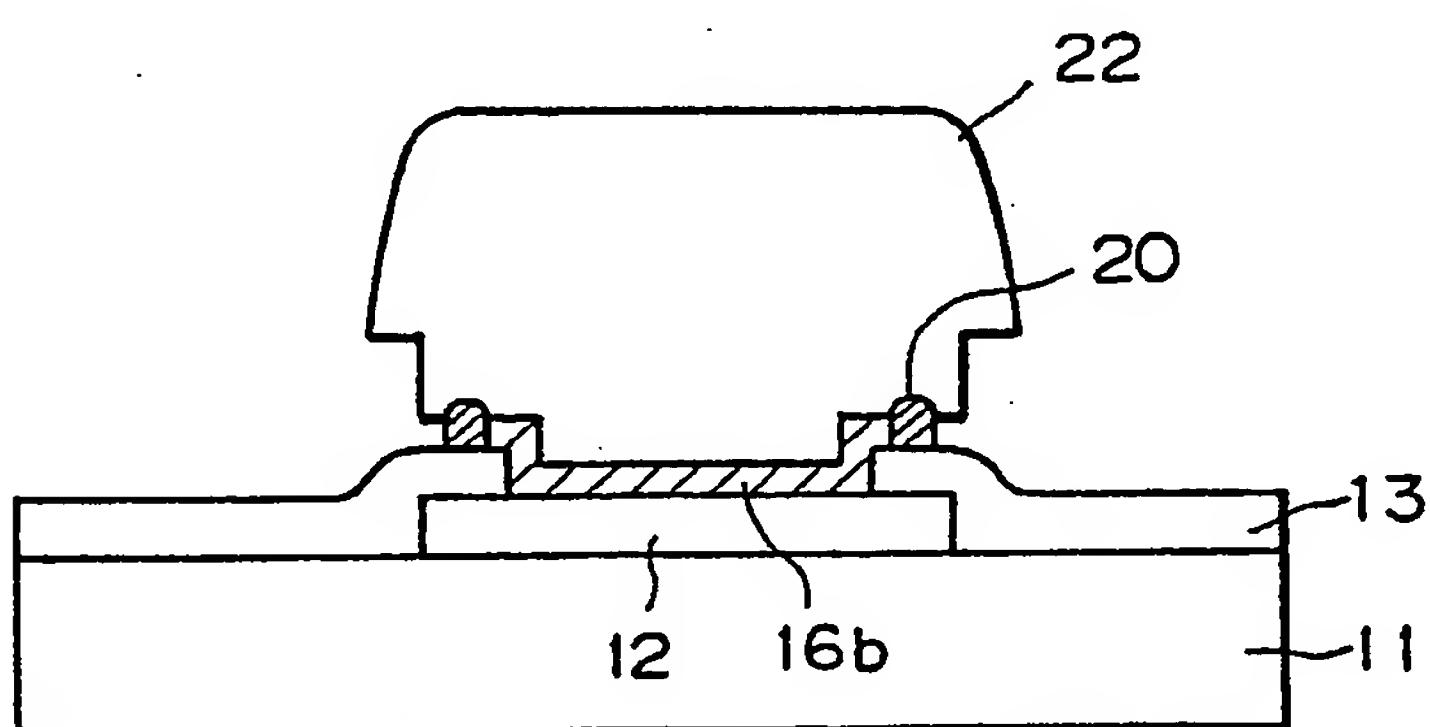


Fig. 3

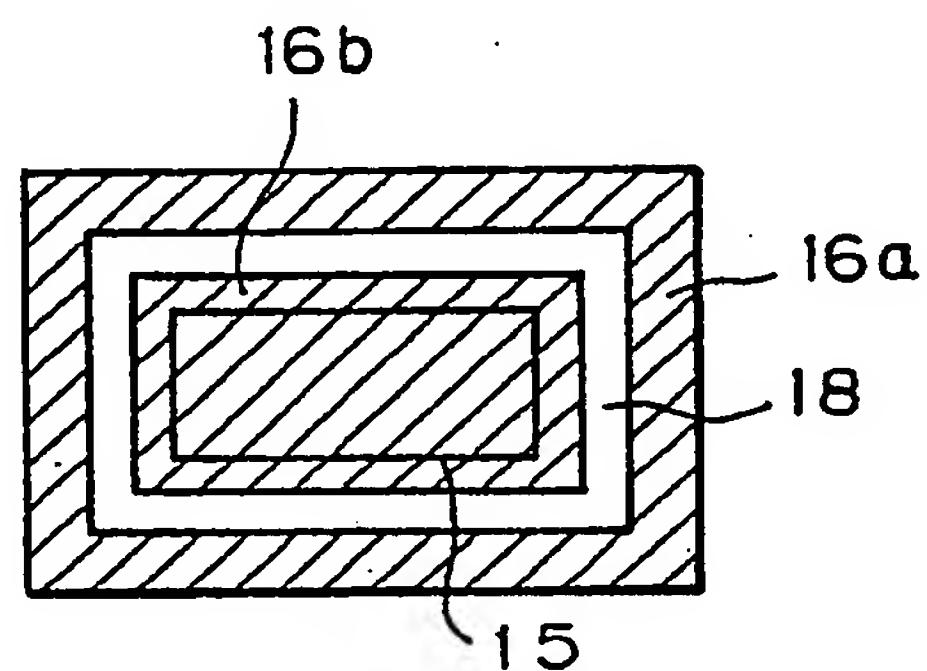


Fig. 4A

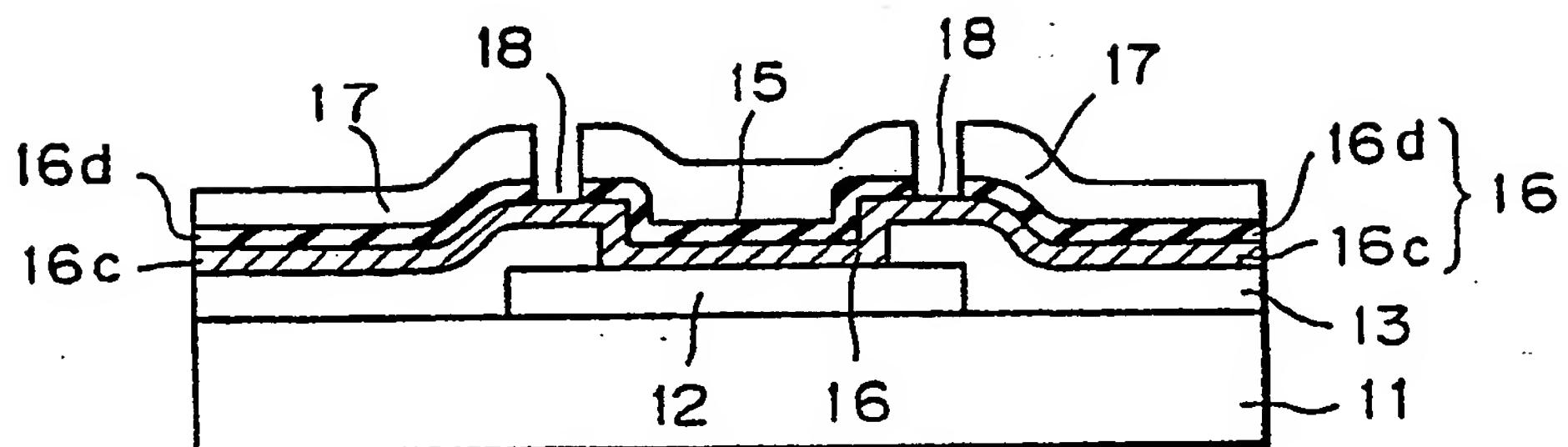


Fig. 4B

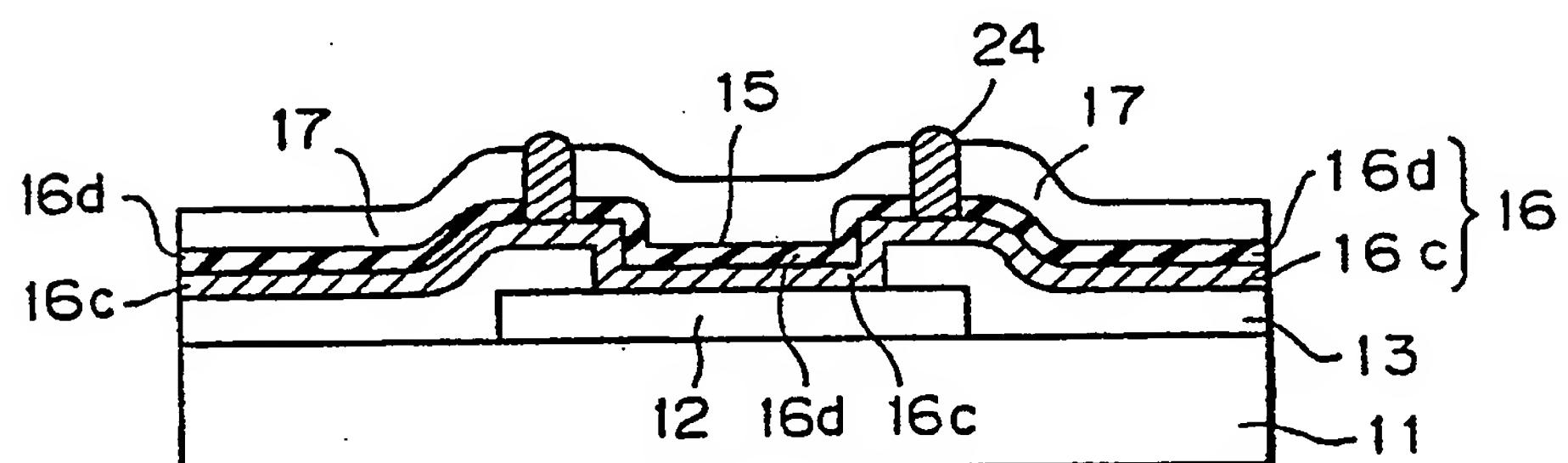
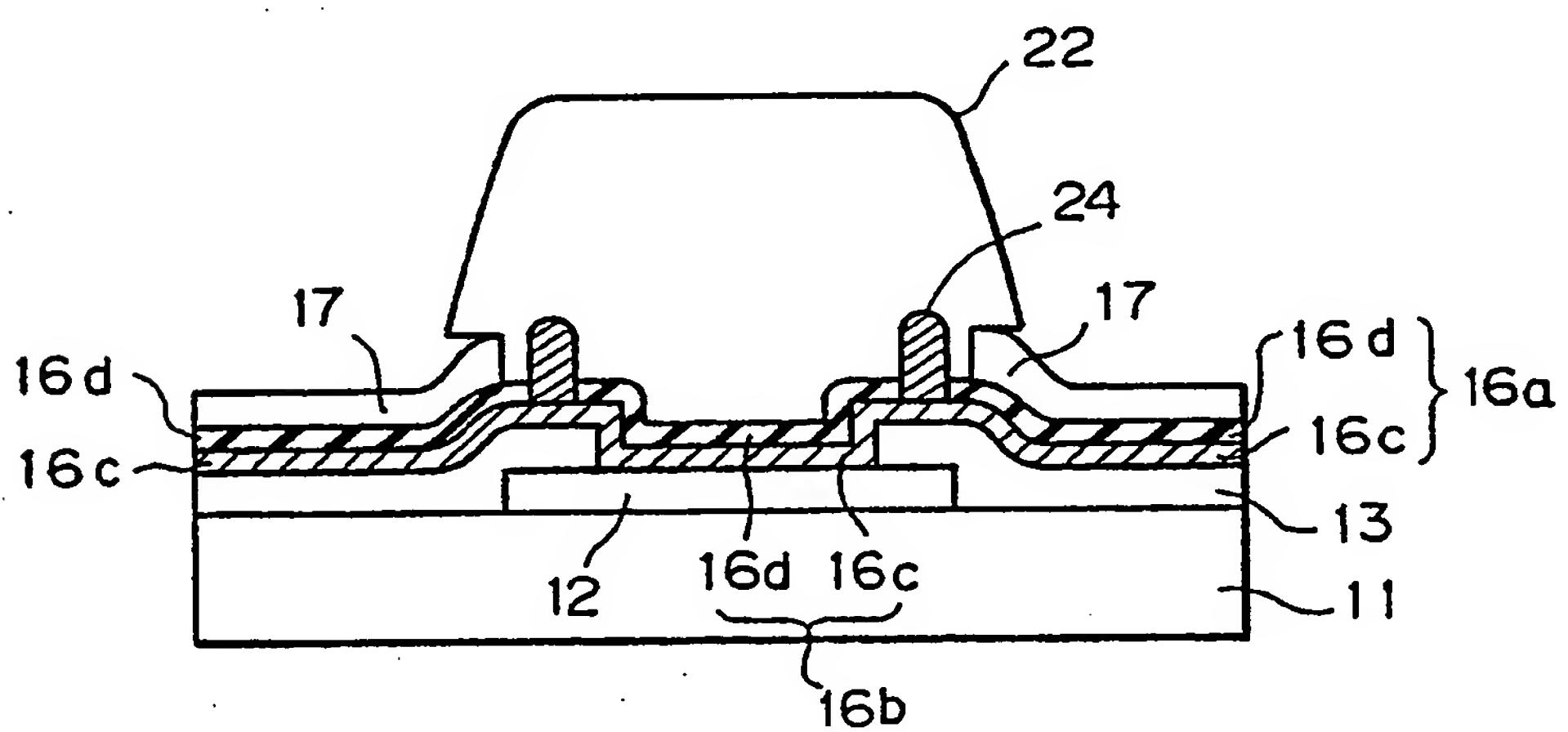
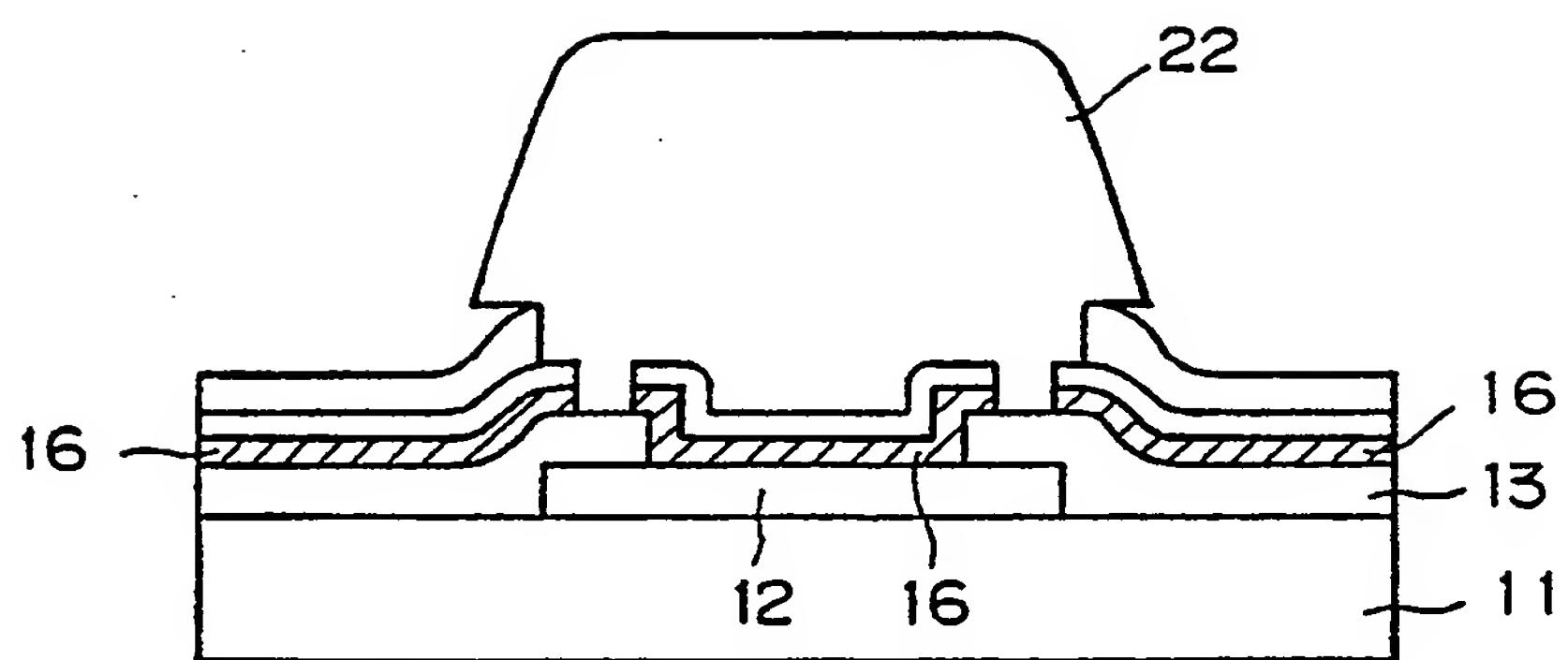


Fig. 4C



*Fig. 5*



*Fig. 6*

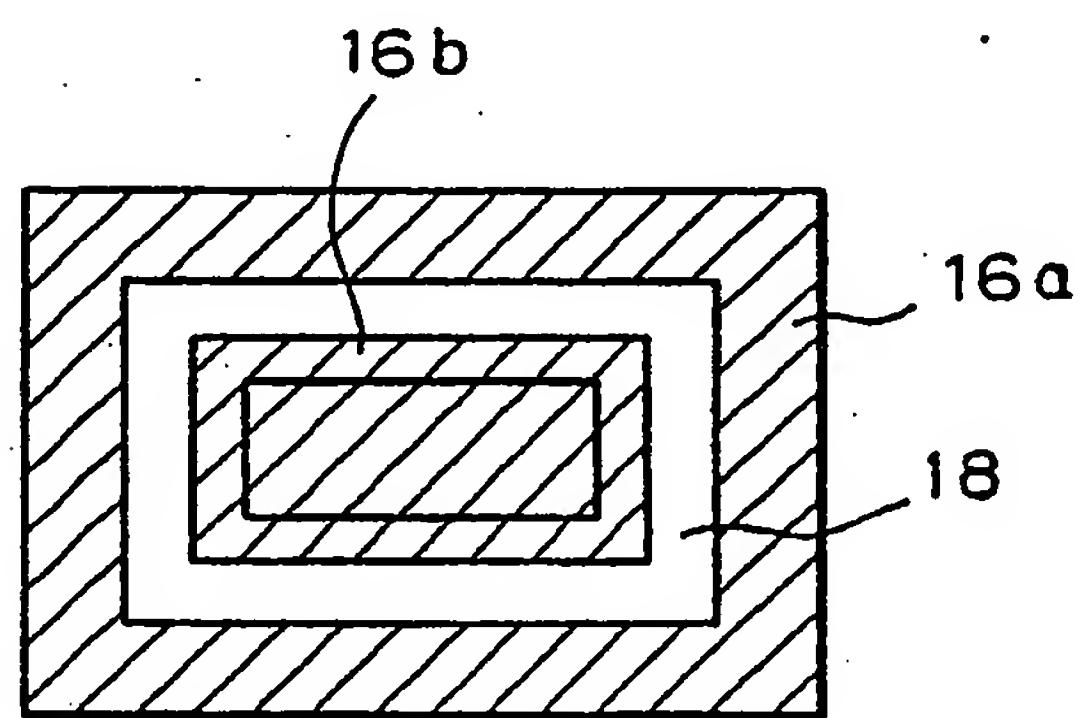


Fig. 7A

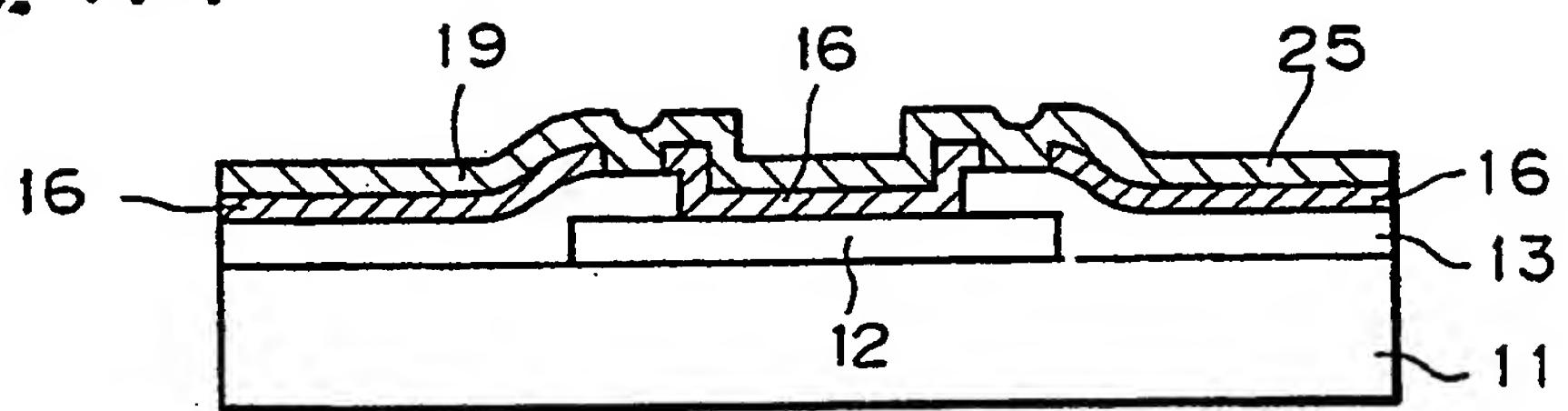


Fig. 7B

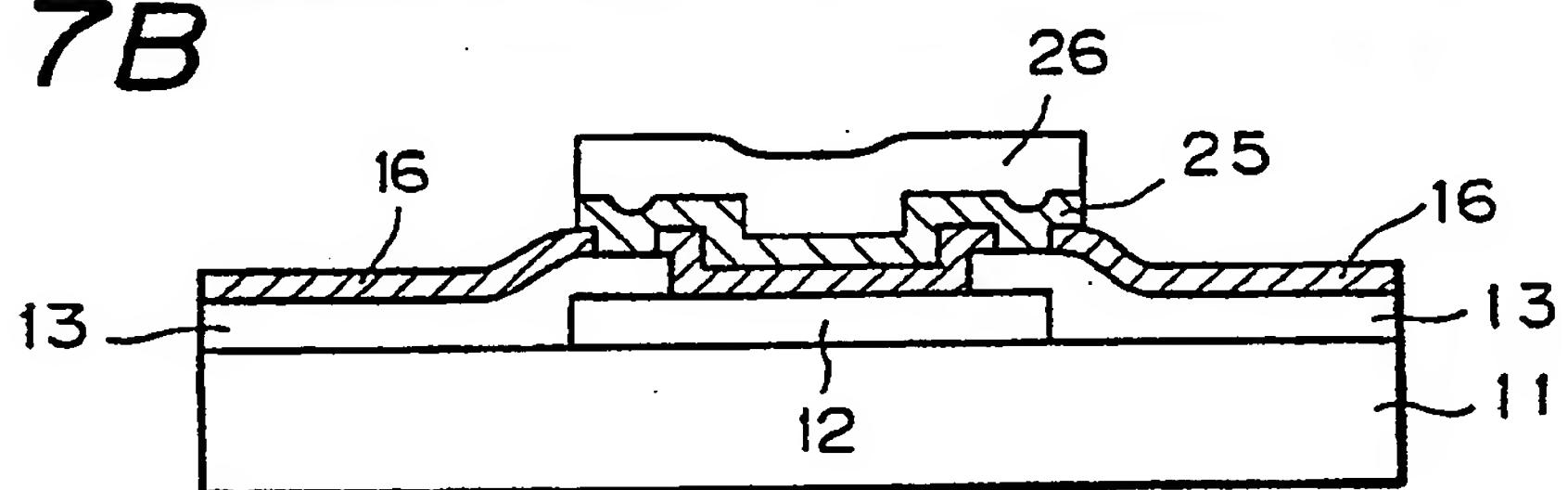


Fig. 7C

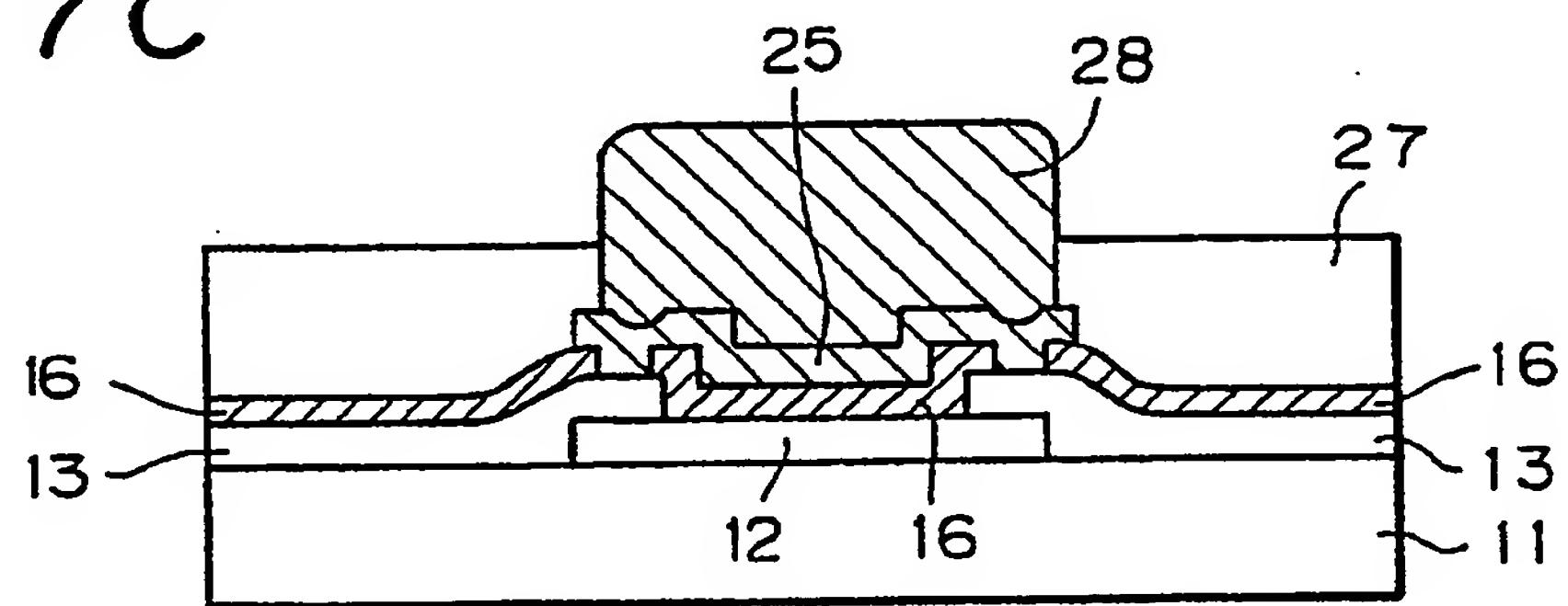
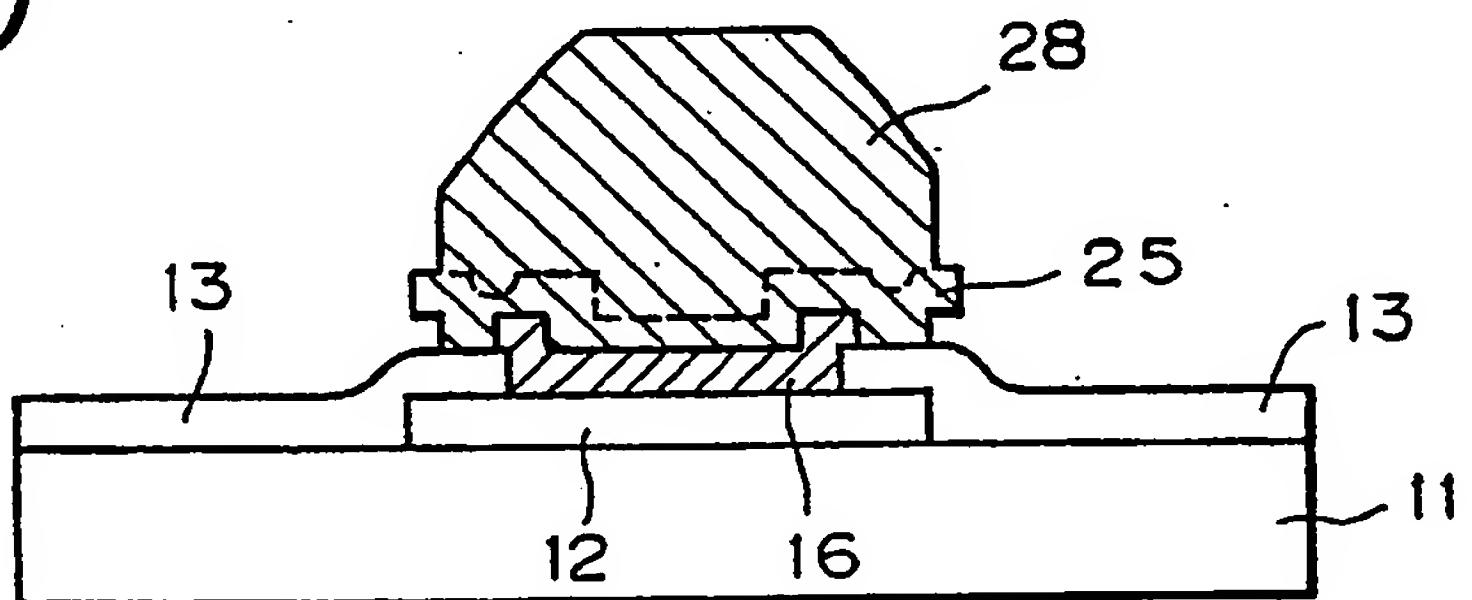
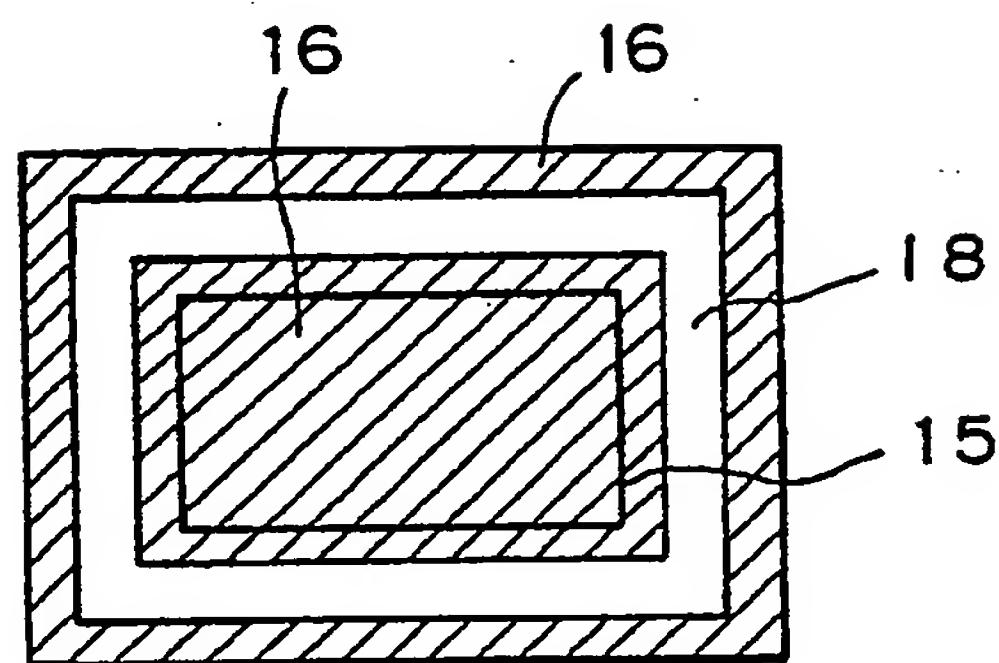


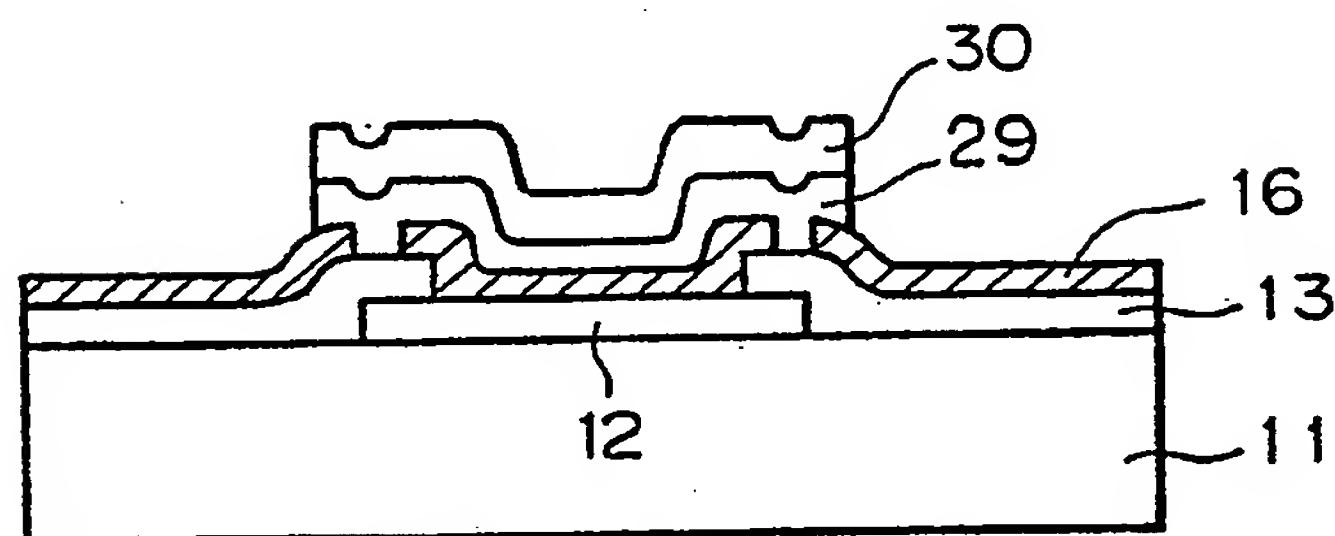
Fig. 7D



*Fig. 8*



*Fig. 9A*



*Fig. 9B*

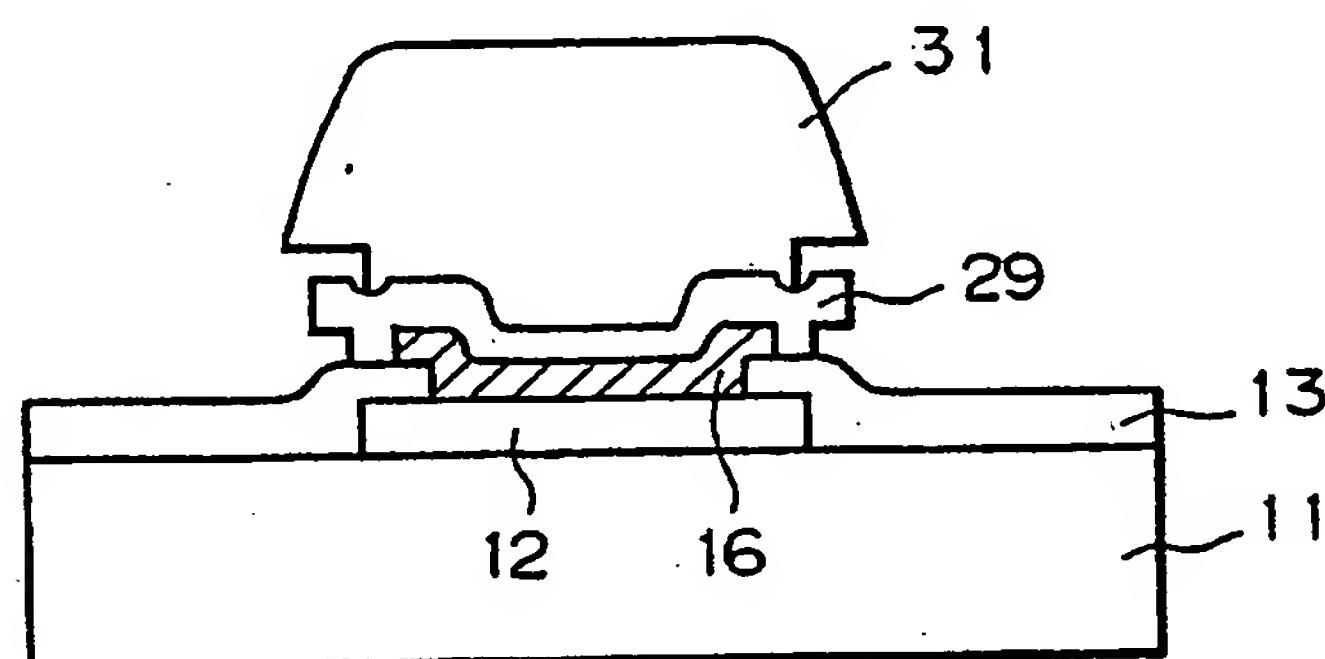


Fig. 10A

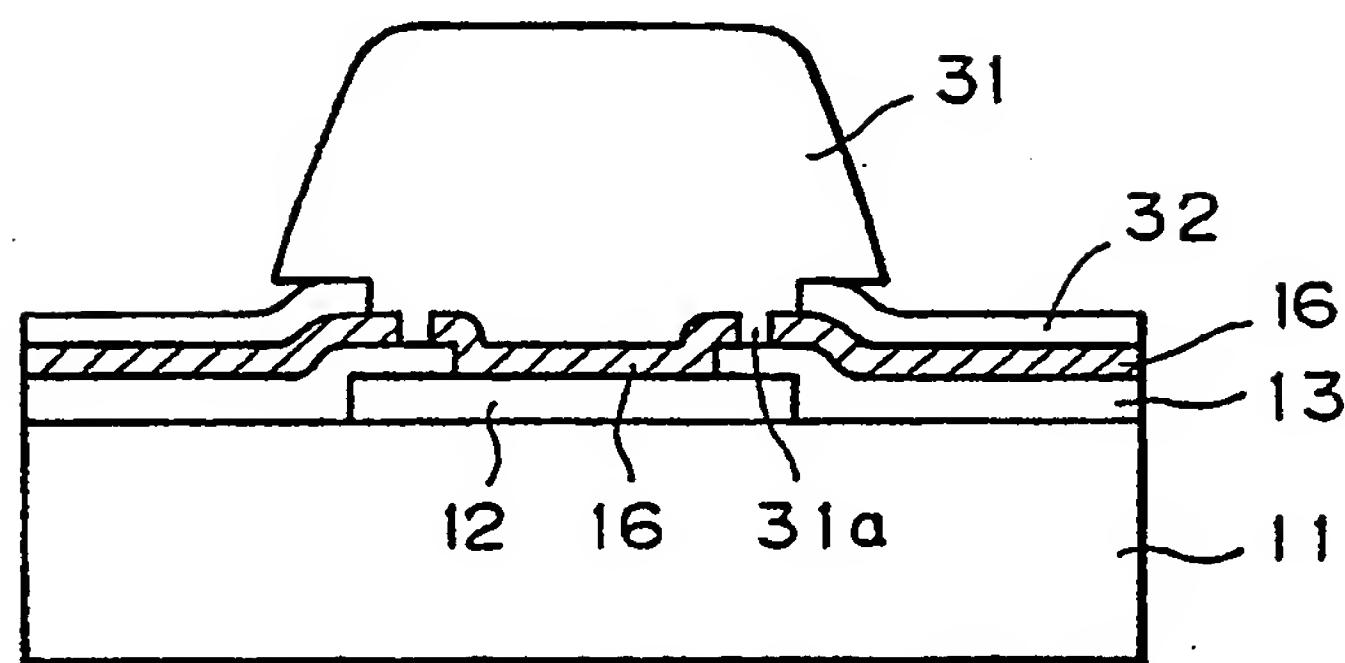
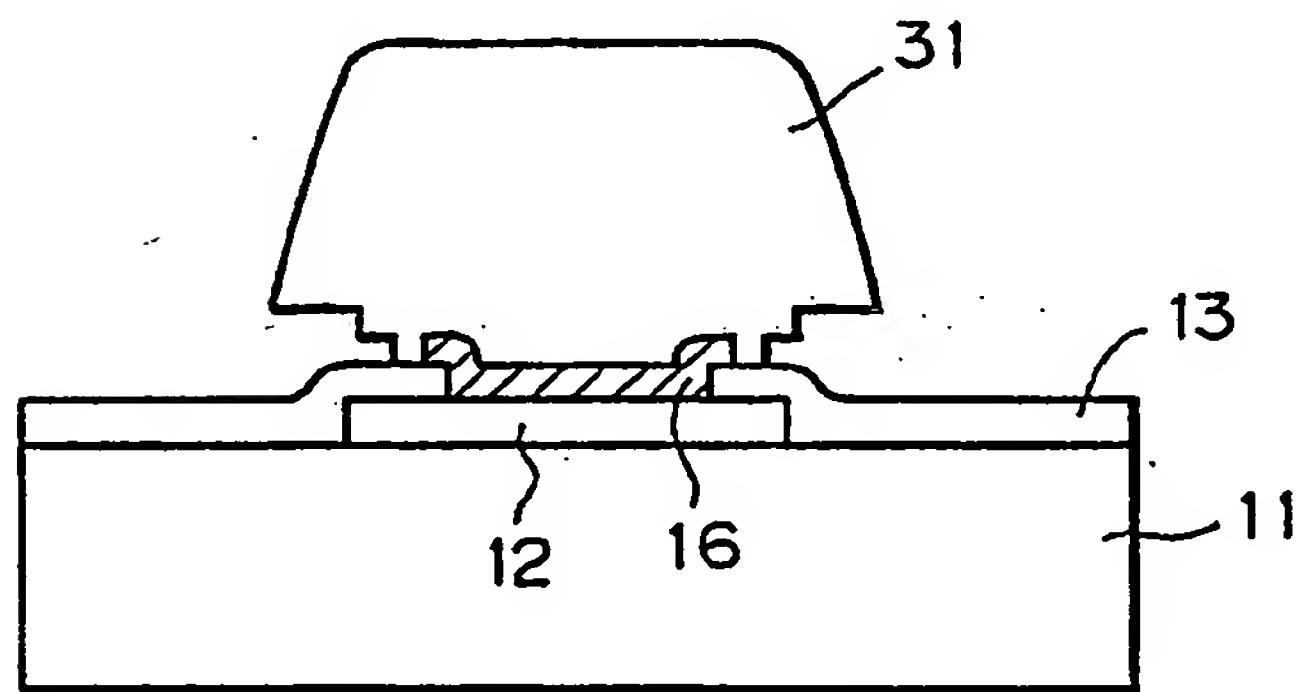


Fig. 10B





EUROPEAN SEARCH REPORT

EP 87 30 7459

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	PROCEEDINGS OF THE 31st ELECTRONIC COMPONENTS CONFERENCE, Atlanta, 11th-13th May 1981, pages 149-155, IEEE; T. KAWANOBE et al.: "Solder bump fabrication by electrochemical method for flip chip interconnection" * Figure 1; table 2 * ---	1-4	H 01 L 23/48 H 01 L 21/60
A	EP-A-0 111 823 (IBM) * Figure 3 * ---	1-4	
A	US-A-4 293 637 (MATSUSHITA ELECTRIC INDUSTRIAL CO.) -----		
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			H 01 L
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	02-12-1987	PHEASANT N.J.	
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